

# QSB Command List

Document Version 1.19

## Product Features:

The QSB is an inexpensive device that provides an interface between a PC and many types of US Digital encoder products. In addition, some variations of the QSB also provide step and direction control signals to an MD2S stepper motor driver and provide 4-bits of digital I/O and 4 analog voltage inputs. There are four different variations in QSB product line.

## QSB Variations:

1. The QSB-S provides one single-ended encoder interface (quadrature, PWM or Analog) or one analog input.
2. The QSB-D provides one differential encoder interface with a 1-bit digital I/O port.
3. The QSB-M provides one single-ended encoder interface (quadrature, PWM or Analog) or one analog input. There is also a 4-bit digital I/O interface, with an option to share 2 I/O lines (step and direction) with an MD2S stepper motor driver interface.
4. The QSB-I provides 4 digital I/O and 4 analog inputs. There is an option to share 2 digital I/O lines with an MD2S stepper motor driver interface.

## Serial Communication:

The commands are sent in RS-232 format over a virtual COM port connection through the USB. The data rate is 230.4 kb/s, 8 data bits, no parity, 1 stop bit, no flow control. The RTS line must be held low and the DTR line must be held high for normal operation. The QSB can be reset with a high-low-high transition on the DTR line.

## Digital I/O:

The digital I/O can be configured as general purpose I/O, as motor step and direction control, or as input/output triggers for the internal quadrature counter. The quadrature counter I/O triggers are listed below:

1. Any of the four digital inputs can be configured to capture the current encoder value upon a positive or negative step change in the digital input state. This feature is configured using the DIG I/O CONFIG register.
2. Digital output, bit 0, can be configured to output a pulse in response to a quadrature counter index, match, underflow or overflow event. The event trigger is enabled in the MDR1 register. The pulse duration is set using the INTERVAL RATE register.



### Command Format:

Commands are sent to the QSB in the format seen in the table below. All commands are composed of a string of ASCII characters terminated by an **EOC** (end of command) sequence. The first field in the command string selects the Command Type; there are three types of commands – **Read**, **Write** and **Stream**. Registers, within the QSB, are configured to support different functions. The second field, the **Register** field, selects the register to read or modify. The **Data** field holds the value for the selected register. The **EOC** field is a command termination sequence. The commands are sent in RS-232 format over a virtual COM port connection through the USB. The data rate is 230.4 kb/s, 8 data bits, no parity, 1 stop bit, no flow control. The RTS line must be held low and the DTR line must be held high for normal operation. The QSB can be reset with a high-low-high transition on the DTR line. NOTE: a backspace character will erase the partially entered command from the command buffer; this is useful when entering commands manually from a terminal.

Command Type[1]	Register[2]	<Data[1..8]>	EOC[1..2]
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Where:

- “Command Type” is a single upper-case ASCII character indicating an ‘R’=read, ‘W’=write ‘S’=Streaming read.
- “Register” is the index number (see below) of the register being addressed. Range is 00 to FF (two upper or lower case ASCII bytes representing a single hex byte)
- “Data” is the optional value to be written to the selected register (eight ASCII hex bytes representing four hex bytes, 00000000 to FFFFFFFF). All data entered, less than 8 bytes in length, will be internally converted to a positive signed long value. Negative values must be entered as a full 4 bytes in two’s-complement format.
- “EOC” is a one to two-byte ASCII character sequence indicating the end of command. The command termination is any single or dual combination of CR and LF characters.

### Command Acknowledgement Format:

All commands will be acknowledged. For read commands, the Data will be the requested register value. For write commands, the returned Data value will be the data received. For example, the response to a MODE register “Quadrature Mode” write command will be the ASCII string “w”, “00”, “00000000”, “!”, followed by the EOR sequence. At the conclusion of the command response, the QSB is ready to accept another command.

Command Response[1]	Register[2]	Data[8]	<TimeStamp[8]>	‘!’	EOR[1..2]
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Where:



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- “Command Response” is a single lower-case ASCII character indicating the Command Type of the last command. An ‘r’=read, ‘w’=write, ‘s’=stream, ‘e’=error, ‘x’=unsupported command.
- “Register” is the index number of the register in the last command. Range is 00 to FF (two ASCII bytes representing a single hex byte).
- “Data” is the value written to, or read from, the selected register (eight ASCII hex bytes representing four hex bytes, 00000000 to FFFFFFFF). Returned data will have added leading 0’s to fill the entire eight bytes. If the error response is returned, Data will be the incorrect data value sent to the QSB; this value was not written to the device.
- “TimeStamp” is the optional timestamp value recorded at the time the data was read. (eight ASCII hex bytes representing four hex bytes, 00000000 to FFFFFFFF). The timestamp represents the number of counts of a 1.9ms internal clock since the last counter reset or power-up time. The value will roll-over if not reset by a user command.
- “!” exclamation character. Always present; it is used for an end-of-line indicator if no end-of-response termination is selected (see EOR).
- “EOR” is the End-Of-Response termination format selected using the EOR TERMINATION register (see below). It could consist of No Termination, CR, LF, TimeStamp or space delimited formatting. No space delimiter precedes the EOR character.



**Command List:**

All functions are activated and configured through the following register settings:

Registers	Reg#	Command Type	Product Type	Data
MODE	00	R, W	-D, -M, -S	<p><u>Encoder Modes</u> This bit-flag parameter sets/reports the type of encoder being used and reports the bit resolution of the PWM encoder (when connected).</p> <p>BITS: B7 B6 B5 B4 B3 B2 B1 B0</p> <p>B1 B0 =00 - QUADRATURE MODE (default) =01 - PWM MODE =10 - ANALOG MODE B2 B3 = Unused B4 = PWM resolution (read only: 1=12-bit, 0=10-bit) B5-7 = Unused</p> <p><b>Data range: 00 – 12</b></p>
DIG I/O	01	R, W, S	-D, -M	<p><u>Digital I/O</u> A read returns the actual state measured at the four digital I/O bit inputs, bit3 – bit0. A write sets the open-drain output state of the four digital I/O bits.</p> <p>BITS: B3 B2 B1 B0</p> <p>1 = Open Drain Output High 0 = Open Drain Output Low</p> <p>In stream mode, a new I/O state is output only if the I/O bit state has changed. A register <i>read</i> will deactivate the streaming mode. Initial state after power up returns to the last saved I/O state (see register 16 command #3).</p> <p><b>Data range: 0 – F</b></p>
DIG I/O CONFIG	02	R, W	-D, -M	<p><u>Digital I/O Configuration</u> Set the direction and interrupt capability of the</p>



				<p>digital I/O pins. All I/O port pins will be set “high” after a write to this configuration register; the user must then set the output states to the desired values by writing to the DIG I/O register.</p> <p>BITS: B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0</p> <p>B3... B0  <u>Interrupt Polarity</u> – I/O bit3...bit0, 1= high-low, 0= low-high  B7 ... B4  <u>Interrupt enable</u> – I/O bit3...bit0, 1=enable, 0=disabled  B11 ... B8  <u>I/O Direction</u> – I/O bit3...bit0, 1=output, 0=input  B12  <u>Trigger pulse enable</u> – 1=enable, 0=disable  When enabled, a trigger event (see register MDR1) causes an output signal on digital I/O bit 0 for a duration specified by the INTERVAL RATE register. The output pulse polarity depends on the initial output state of digital I/O bit 0. An INTERVAL RATE value of 0 only toggles the digital output. The feature is initially disabled; however, the current parameter state is saved with the save-parameters command.</p> <p><b>NOTE:</b> There is only one I/O input interrupt implemented; it will load the current encoder value into the CAPTURE register. I/O BITS 0 – 4 can all trigger this interrupt. Be careful if the motor drive is enabled, it uses I/O bits 1 and 2.</p> <p><b>Data range: 0000 - 1FFF</b></p>
MDR0	03	R, W	-D, -M, -S	<p><u>Counter Mode Register 0</u>  The MDR0 (Mode Register 0) is an 8-bit read/write register that sets up the operating mode for the internal LS7366R counter. The following is a breakdown of the MDR0 bits:</p> <p>BITS: B7 B6 B5 B4 B3 B2 B1 B0</p> <p>B1 B0</p>



				<p>= 00: non-quadrature count mode. (A = clock, B = direction).</p> <p>= 01: x1 quadrature count mode (one count per quadrature cycle).</p> <p>= 10: x2 quadrature count mode (two counts per quadrature cycle).</p> <p>= 11: x4 quadrature count mode (four counts per quadrature cycle).</p> <p><b>B3 B2</b></p> <p>= 00: free-running count mode.</p> <p>= 01: single-cycle count mode. The counter is disabled with a carry or borrow (32-bit counter) and re-enabled with reset or load.</p> <p>= 10: range-limit count mode. Up and down count-ranges are limited between DTR and zero, respectively; counting freezes at these limits but resumes when direction reverses.</p> <p>= 11: modulo-n count mode. The DTR register is used as the counter rollover value.</p> <p><b>B5 B4</b></p> <p>= 00: disable index.</p> <p>= 01: configure index as the "load CNTR" input (transfers DTR to CNTR).</p> <p>= 10: configure index as the "reset CNTR" input (clears CNTR to 0).</p> <p>= 11: configure index as the "load OTR" input (transfers CNTR to OTR).</p> <p><b>B6</b></p> <p>= 0: Asynchronous Index</p> <p>= 1: Synchronous Index (overridden in non-quadrature mode)</p> <p><b>B7</b> (<i>note: The filter clock input is 24MHz</i>)</p> <p>= 0: Filter clock division factor = 1</p> <p>= 1: Filter clock division factor = 2</p> <p><b>Data range: 00 - FF</b></p>
MDR1	04	R, W	-D, -M, -S	<p><b>Counter Mode Register 1</b></p> <p>The MDR1 (Mode Register 1) is an 9-bit read/write register which is appended to MDRO</p>



				<p>for additional modes.</p> <p>BITS: B8 B7 B6 B5 B4 B3 B2 B1 B0</p> <p>B1 B0 = Reserved – always set to 00 (32-bit counter mode only)</p> <p>B2  = 0: Enable counting  = 1: Disable counting</p> <p>B3: Encoder Index Polarity  = 0: Non invert index (USD encoder default)  = 1: Invert Index</p> <p>B4 Trigger/Capture on Index  = 0: Disable  = 1: Enable</p> <p>B5 Trigger on Match  = 0: Disable  = 1: Enable</p> <p>B6 Trigger on Underflow  = 0: Disable  = 1: Enable</p> <p>B7 Trigger on Overflow  = 0: Disable  = 1: Enable</p> <p>B8 Counter Direction  =0: Count-up mode (quad encoder only)  =1: Count-down mode (quad encoder only)</p> <p>NOTE: Capture-on-x causes the current quadrature counter value to be captured on the event. Also, an output pulse is generated, on Digital I/O bit 0, if a trigger-on-x flag is set. Bit-12, of the I/O Config register, must also be enabled in both cases for a capture or output pulse to occur.</p>
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				<b>Data range: 00 - 1FF</b>
CAPTURE	05	R, S	-D, -M, -S	<u>Counter Capture Register</u> This register contains the value of the quadrature state counter captured during a index capture event (see MDR1) or the encoder value captured at an interrupt event on a digital I/O bit. In streaming mode, a new value is output when the register value changes. A read of this register will cancel the streaming mode if enabled.  <b>Data range: 00000000 - FFFFFFFF</b>
STR	06	R, S	-D, -M, -S	<u>Counter Status Register</u> Stores count related status information.  BITS: B7 B6 B5 B4 B3 B2 B1 B0  B7 = CY - Carry (CNTR overflow) latch B6 = BW - Borrow (CNTR underflow) latch B5 = CMP - Compare (CNTR = DTR) latch B4 = IDX - Index latch B3 = CEN - Count enable status: 0: counting disabled, 1: counting enabled B2 = PLS - Power loss indicator latch; set upon power up B1 = U/D - Count direction indicator: 0: count down, 1: count up. B0 = S - Sign bit. Set to 1 on underflow, set to 0 on overflow.  In streaming mode, a new value is output when the register value changes. A read of this register will cancel the streaming mode if enabled.  <b>Data range: 00 - FF</b>
OTR	07	R	-D, -M, -S	<u>Output Transfer Register</u> The OTR is a drop-off site for instantaneous CNTR data which can then be read without interfering with the counting process.  <b>Data range: 00000000 - FFFFFFFF</b>
DTR	08	R, W	-D, -M, -S	<u>Input Transfer Register</u> The DTR data can be transferred into the counter (CNTR) under program control or by hardware index signal. In compare operations, whereby



				compare flag is set, the DTR is compared with the CNTR.  <b>Data range: 00000000 - FFFFFFFF</b>
CLEAR REG	09	W	-D, -M, -S	<u>Clear Selected Counter Registers</u> The following registers can be cleared to 0: 0 = MDR0 1 = MDR1 2 = CNTR 3 = STR  <b>Data range: 0 – 3</b>
LOAD REG	0A	W	-D, -M, -S	<u>Load Selected Registers</u> The following registers can be loaded: 0 = Transfer DTR to CNTR 1 = Transfer CNTR to OTR  <b>Data range: 0 – 1</b>
THRESHOLD	0B	R, W	-D, -M, -S	<u>Encoder Count Threshold</u> This sets the absolute count threshold, between the previous count value and the current count value, before a new output value is reported at the selected interval rate. A value of 0 will output all values at the selected interval rate.  <b>Data range: 0000 - FFFF</b>
INTERVAL RATE	0C	R, W	-D, -M, -S	<u>Data Output Interval Rate</u> This sets the data output display rate in 1.9ms steps (1/512 Hz clock). A value of 0xFFFF will disable the streaming output. A value of 0x0000 would output the data as fast as possible. For example, a value of 1 = 1.9ms delay, 2 = 3.8ms delay and so on.  <b>Data range: 0000 – FFFF</b>
TIME STAMP	0D	R, W	-D, -M, -S	<u>Time Stamp Value</u> The time stamp counter is a 32-bit counter incremented every 1.9ms (1/512Hz clock). It is used to time-stamp data that is saved in the on board RAM chip. This counter is cleared on a power-cycle or by this command; write a 1 to this register to clear the timer. A read will return the



				current 32-bit time stamp value. If not reset, a counter rollover will happen every 94.5 days.  <b>Data range: 00000000-FFFFFFFF</b>
READ ENCODER	0E	R, S	-D, -M, -S	<u>Read the Current Encoder Value</u> Read the value of the encoder. If in Quadrature mode, the encoder value will be returned as a 32-bit value. If in PWM mode, a 12/10-bit (4 character, leading 0) value will be returned. If in Analog mode, a 10-bit value will be returned. In stream mode, the new encoder value is output at a rate set by the INTERVAL RATE and THRESHOLD parameters. A read of the encoder value will disable the streaming mode.  <b>Data range: 00000000 – FFFFFFFF</b>
MD STEP RATE	0F	R, W	-M	<u>MD2: Motor Step Rate</u> Set motor step rate from 32 – 13000 steps/second. Motor rate will change in increments of 16 steps/second. (hex 20 – 32C8 steps/second)  <b>Data range: 00000020 – 000032C8</b>
MD ACCEL	10	R, W	-M	<u>MD2: Motor Step Acceleration</u> Set motor step acceleration from 64 – 360000 steps/second <sup>2</sup> . Motor acceleration will change in increments of 16 steps/second <sup>2</sup> . (0x40 – 0x57E40 steps/second <sup>2</sup> )  <b>Data range: 00000040 – 00057E40</b>
MD MOVE STEPS	11	R, W	-M	<u>MD2: Motor Steps to Move</u> Number of steps to move. Range + – (2 <sup>31</sup> )-1 (negative value indicates direction)  <b>Data range: 80000001 to 7FFFFFFF</b>
MD JOG RATE	12	R, W	-M	<u>MD2: Motor Jog Rate</u> Motor rate in steps/second. Motor rate will change in increments of 16 steps/second. Range -13000 to 13000. (hex +- 32C8)  <b>Data range: FFFCD38 to 000032C8</b>
MD STATUS	13	R, S	-M	<u>MD2: Request Motor Movement Status</u>



				<p>BITS: B4 B3 B2 B1 B0</p> <p>B0 = Done/Ready  B1 = Moving  B2 = Paused  B3 = Jogging  B4 = Motor Enabled</p> <p>In stream mode, the new MD STATUS is output upon a state change. A read of MD STATUS will cancel the streaming mode.</p> <p><b>Data range: 0 – 1F</b></p>
VERSION	14	R	-D, -M, -S	<p><u>QSB SN, Product Type and Firmware Version</u>  Returns the 5-digit device serial number, one-digit product type and two-digit firmware version. In the eight digit response, the first five most significant digits are the serial number, the next digit is the product type and the last two digits are the firmware version.</p> <p>Product type code:  0 = QSB-D  1 = QSB-M  2 = QSB-S  3 = QSB-I (future product)</p> <p>Example, 00001201 = SN: 00001, Type: QSB-S, Version: 01</p> <p><b>Data range: 00000000 - FFFFFFFF</b></p>
EOR	15	R, W	-D, -M, -S	<p><u>EOR (End Of Response) Termination and Formatting</u>  This command defines the type of formatting for the command response termination. Each feature is enabled with a bit=1 or disabled with a bit=0. The default value is: 0x0b.</p> <p>BITS: B3 B2 B1 B0</p>



				<p>B0 = Line Feed          B1 = Carriage Return          B2 = 4-byte Time Stamp appended to response          B3 = Spaces between returned fields</p> <p><b>Data range: 0 – F</b></p>
COMMAND	16	W	-D, -M, -S	<p><u>Execute QSB Command Function</u></p> <p>Data=1 : -D and -S</p> <p>Data=all: -M</p> <p>0 = Motor is immediately stopped. Encoder, Digital I/O and MD Status streaming data outputs are deactivated. Motor drive status is set to the inactive state; digital I/O port is returned to the last saved state (see command #3 below).</p> <p>1 = Deactivate Encoder, Digital I/O and MD Status streaming data outputs.</p> <p>2 = Activate motor drive mode; digital I/O bits 1 and 2 are reserved for motor drive.</p> <p>3 = Save Parameters: save register# 00 – 04, 08, 0B, 0C, 0F – 12, 15. Save motor drive enable state flag (command #2 above).</p> <p>4 = Motor Stop - Stop the motor using the MD ACCEL rate.</p> <p>5 = Motor Quit -Immediately stop the motor.</p> <p>6 = Motor Pause - Pause the motor using the MD ACCEL rate.</p> <p>7 = Motor Resume - Resume motor operation if previously stopped using the Motor Pause command. Use the programmed motor acceleration.</p> <p>8 = Motor Move – Move the selected number of MD MOVE STEPS.</p> <p>9 = Motor Jog – Jog at the selected MD JOG RATE.</p>



				<b>Data range: 0 – 9</b>



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