QSB Command List

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Changelog

Date	Comment(s)
6/10/2013	Version 1.22 - Added command to support multiple baud rates.
3/26/2014	Version 1.23 - Removed references to QSB-I product.
3/01/2016	Version 1.24 - Reworded definition of index synchronization in register MDR0 bit 6.
8/15/2017	Version 1.25 – Made clarifications to various sections of the document. Added sample commands after each register definition.

Product Features:

The QSB is an inexpensive device that provides an interface between a PC and many types of US Digital encoder products. In addition, some variations of the QSB provide step and direction control signals to an MD2S stepper motor driver and provide 4-bits of digital I/O and an analog voltage input. There are three different variations in QSB product line.

QSB Variations:

1. The QSB-S provides one single-ended encoder interface; selectable as a quadrature, step/direction, PWM or analog input.
2. The QSB-D provides one differential encoder interface with a 1-bit digital I/O port.
3. The QSB-M provides one single-ended encoder interface; selectable as a quadrature, step/direction, PWM or analog input. There is also a 4-bit digital I/O interface, with an option to attach two selected output lines (step and direction) with an MD2S stepper motor driver interface.

Serial Communication:

The commands are sent in RS-232 format over a virtual COM port connection through the USB. The default factory data rate is 230.4 kb/s, 8 data bits, no parity, 1 stop bit, no flow control. The RTS line must be held low and the DTR line must be held high for normal operation. The QSB can be reset with a high-low-high transition on the DTR line.

Digital I/O:

The digital I/O can be configured as general purpose I/O, as motor step and direction control, or as input/output triggers for the internal encoder step counter. The counter's I/O triggers are listed below:

1. Any of the four digital inputs can be configured to capture the current encoder count value upon a positive or negative step change in the digital input state. This feature is configured using the DIG I/O CONFIG register.
2. Digital output, bit 0, can be configured to output a pulse in response to a quadrature counter index, match, underflow or overflow event. The event trigger is enabled in the MDR1 register. The pulse duration is set using the INTERVAL RATE register.

Command Format:

Commands are sent to the QSB in the format seen in the table below. All commands are composed of a string of ASCII characters terminated by an **EOC** (end of command) sequence. The first field in the command string selects the Command Type; there are three types of commands – **R**ead, **W**rite and **S**tream. Registers, within the QSB, are configured to support different functions. The second field, the **Register** field, selects the register to read or modify. The **Data** field holds the value for the selected

register. The **EOC** field is a command termination sequence. The commands are sent in RS-232 format over a virtual COM port connection through the USB. The default data rate is 230.4 kb/s, 8 data bits, no parity, 1 stop bit, no flow control. The RTS line must be held low and the DTR line must be held high for normal operation. The QSB can be reset with a high-low-high transition on the DTR line. NOTE: a backspace character will erase a partially entered command from the command buffer; this is useful when entering commands manually from a terminal.

Command Type[1]	Register[2]	<Data[1..8]>	EOC[1..2]

Where:

- "Command Type" is a single upper-case ASCII character indicating an 'R'=read, 'W'=write 'S'=Streaming read.
- "Register" is the index number (see below) of the register being addressed. Range is 00 to FF (two upper or lower case ASCII bytes representing a single hex byte)
- "Data" is the optional value to be written to the selected register (eight ASCII hex bytes representing four hex bytes, 00000000 to FFFFFFFF). All data entered, less than 8-bytes in length, will be internally converted to a positive signed long value; leading zeros are ignored. Negative values must be entered as a full 4-bytes in two's-complement format.
- "EOC" is a one to two-byte ASCII character sequence indicating the end of command. The command termination is any single or dual combination of CR and LF characters.

Command Acknowledgement Format:

All commands will be acknowledged. For read commands, the Data will be the requested register value. For write commands, the returned Data value will be the data received. For example, the response to a MODE register "Quadrature Mode" write command will be the ASCII string "w", "00", "00000000", "!", followed by the EOR sequence. At the conclusion of the command response, the QSB is ready to accept another command.

Command Response[1]	Register[2]	Data[8]	<TimeStamp[8]>	'!'	<EOR[1..2]>

Where:

- "Command Response" is a single lower-case ASCII character indicating the Command Type of the last command. An 'r'=read, 'w'=write, 's'=stream, 'e'=error, 'x'=unsupported command.
- "Register" is the index number of the register in the last command. Range is 00 to FF (two ASCII bytes representing a single hex byte).
- "Data" is the value written to, or read from, the selected register (eight ASCII hex bytes representing four hex bytes, 00000000 to FFFFFFFF). Returned data will have added leading 0's

to fill the entire eight bytes. If the error response is returned, Data will be the incorrect data value sent to the QSB; this value was not written to the device.

- "TimeStamp" is the optional timestamp value recorded at the time the data was read. (eight ASCII hex bytes representing four hex bytes, 00000000 to FFFFFFFF). The timestamp represents the number of counts of a 1.9ms internal clock since the last counter reset or power-up time. The value will roll-over if not reset by a user command.
- "!" exclamation character. Always present; it is used for an end-of-line indicator if no end-of-response termination is selected (see EOR).
- "EOR" is the End-Of-Response termination format selected using the EOR TERMINATION register (see below). It could consist of No Termination, CR, LF, TimeStamp or space delimited formatting. No space delimiter precedes the EOR character.

Special Analog Measurement Command Acknowledgement Data Format:

The QSB firmware will allow for combined analog and digital I/O signal measurements for higher data speeds; this could be used for an Oscilloscope application. The Analog measurement mode is activated by setting the ANALOG MODE value in the MODE register. The measurements could then be streamed. The data output rate and format is controlled by the registers: THRESHOLD, INTERVAL RATE and EOR. For analog measurements, the Data section of the Command Acknowledgement format (seen above), is replaced with the 4-byte (eight-character) Data packet shown below:

Time Stamp [16-bits]	Digital I/O [4-bits]	0 0	Analog [10-bits]

Where:

- Time Stamp is a 16-bit 500us counter value (rollover every 32 seconds)
- Digital I/O is the QSB's bit3 – bit0 digital input values
- 00 is two zero bit values
- Analog is the 10-bit Analog input value representing a 0 – 5V input.

Command List:

All functions are activated and configured through the following register settings:

Registers	Reg#	Command Type	Product Type	Data
MODE	00	R, W	-D, -M, -S	Encoder Modes This parameter sets/reports the type of encoder being used and reports the bit resolution of a US Digital PWM encoder (when connected). BITS: B7 B6 B5 B4 B3 B2 B1 B0 B1 B0 =00 - QUADRATURE MODE (*) =01 - PWM MODE =10 - ANALOG MODE (**) B3 B2 = Unused B4 = PWM resolution (read only: 1=12-bit, 0=10-bit) B7-B5 = Unused (*) Step/Direction count also programmable (**) See: "Special Analog Measurement Command Acknowledgement Format" section **Data range: 00 – 12** **Example: Set PWM Encoder Mode, W0001**
DIG I/O	01	R, W, S	-D, -M	Digital I/O A read returns the actual state measured at the four digital I/O bit inputs, bit3 – bit0. A write sets the open-drain output state of the four digital I/O bits. BITS: B3 B2 B1 B0 1 = Open Drain Output High (internal pull-up) 0 = Open Drain Output Low In stream mode, a new I/O state is output only if the I/O bit state has changed. A register *read* will

				deactivate the streaming mode. **Data range: 0 – F** **Example: Stream Digital I/O Inputs: S01**
DIG I/O CONFIG	02	R, W	-D, -M	Digital I/O Configuration Set the direction and interrupt capability of the digital I/O pins. All I/O port pins will be set "high" after a write to this configuration register; the user must then set the output states to the desired values by writing to the DIG I/O register. BITS: B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 B3 - B0 Interrupt Polarity – I/O bit3…bit0, 1= high-low, 0= low-high B7 - B4 Interrupt enable – I/O bit3…bit0, 1=enable, 0=disabled B11 - B8 I/O Direction – I/O bit3…bit0, 1=output, 0=input B12 Trigger pulse enable – 1=enable, 0=disable When enabled, a trigger event (see register MDR1) causes an output signal on digital I/O bit 0 for a duration specified by the INTERVAL RATE register. The output pulse polarity depends on the initial output state of digital I/O bit 0. An INTERVAL RATE value of 0 only toggles the digital output. **NOTE**: There is only one I/O input interrupt implemented; it will load the current encoder value into the CAPTURE register. I/O BITS 0 – 4 can all trigger this interrupt. Be careful if the motor drive is enabled, it uses I/O bits 1 and 2. **Data range: 0000 - 1FFF** **Example: Set All I/O as Outputs, W02F00**
MDR0	03	R, W	-D, -M, -S	Counter Mode Register 0 The MDR0 (Mode Register 0) is an 8-bit read/write register that sets up the operating

				mode for the internal LS7366R counter. The following is a breakdown of the MDR0 bits: BITS: B7 B6 B5 B4 B3 B2 B1 B0 B1 B0 = 00: non-quadrature count mode. (A = clock, B = direction). = 01: x1 quadrature count mode (one count per quadrature cycle). = 10: x2 quadrature count mode (two counts per quadrature cycle). = 11: x4 quadrature count mode (four counts per quadrature cycle). B3 B2 = 00: free-running count mode. = 01: single-cycle count mode. The counter is disabled with a carry or borrow (32-bit counter) and re-enabled with reset or load. = 10: range-limit count mode. Up and down count-ranges are limited between DTR and zero, respectively; counting freezes at these limits but resumes when direction reverses. = 11: modulo-n count mode. The DTR register is used as the counter rollover value. B5 B4 = 00: disable index. = 01: configure index as the "load CNTR" input (transfers DTR to CNTR). = 10: configure index as the "reset CNTR" input (clears CNTR to 0). = 11: configure index as the "load OTR" input (transfers CNTR to OTR). B6 = 0: Asynchronous Index – Applied to any phase relationship of A and B inputs. (Asynchronous index mode is set in non-quadrature modes.) = 1: Synchronous Index – Index is applied during a minimum of a quarter cycle of both A and B inputs high or both A and B inputs low.

				B7 (*note: The filter clock input is 24MHz*) = 0: Filter clock division factor = 1 = 1: Filter clock division factor = 2 **Data range: 00 – FF** **Example: Sync Index, Reset on Index, Free Running, X4 mode, W0363**
MDR1	04	R, W	-D, -M, -S	Counter Mode Register 1 The MDR1 (Mode Register 1) is an 9-bit read/write register which is appended to MDR0 for additional modes. BITS: B8 B7 B6 B5 B4 B3 B2 B1 B0 B1 B0 = Reserved – always set to 00 (32-bit counter mode only) B2 = 0: Enable counting = 1: Disable counting B3: Encoder Index Polarity = 0: Non invert index (USD encoder default) = 1: Invert Index B4 Trigger/Capture on Index = 0: Disable = 1: Enable B5 Trigger on Match = 0: Disable = 1: Enable B6 Trigger on Underflow = 0: Disable = 1: Enable B7 Trigger on Overflow = 0: Disable = 1: Enable B8 Counter Direction =0: Count-up mode (quad encoder only)

				=1: Count-down mode (quad encoder only) NOTE: Capture-on-index or capture-on-interrupt events cause the current counter value to be copied to the CAPTURE register. Also, an output pulse is generated, on Digital I/O bit 0, if a trigger flag is set. Bit-12, of the DIG I/O CONFIG register, must also be enabled in both cases for an output pulse to occur. **Data range: 00 - 1FF** **Example: Count Up No Triggers, W04000**
CAPTURE	05	R, S	-D, -M, -S	Counter Capture Register This register contains the value of the quadrature state counter captured during an index capture event (see MDR1) or the value captured at an interrupt event on a digital I/O bit. In streaming mode, a new value is output when the register value changes. A read of this register will cancel the streaming mode if enabled. **Data range: 00000000 – FFFFFFFF** **Example: Read Captured Value, R05**
STR	06	R, S	-D, -M, -S	Counter Status Register Stores count related status information. BITS: B7 B6 B5 B4 B3 B2 B1 B0 B7 = CY - Carry (CNTR overflow) latch B6 = BW - Borrow (CNTR underflow) latch B5 = CMP - Compare (CNTR = DTR) latch B4 = IDX - Index latch B3 = CEN - Count enable status: 0: counting disabled, 1: counting enabled B2 = PLS - Power loss indicator latch; set upon power up B1 = U/D - Count direction indicator: 0: count down, 1: count up. B0 = S - Sign bit. Set to 1 on underflow, set to 0 on overflow. In streaming mode, a new value is output when the register value changes. A read of this register

				will cancel the streaming mode if enabled. **Data range: 00 – FF** **Example: Read Status Register, R06**
OTR	07	R	-D, -M, -S	Output Transfer Register The OTR is a drop-off site for instantaneous counter (CNTR) data which can then be read without interfering with the counting process. **Data range: 00000000 – FFFFFFFF** **Example: Read OTR Register, R07**
DTR	08	R, W	-D, -M, -S	Input Transfer Register The DTR data can be transferred into the counter (CNTR) under program control or by hardware index signal. In compare operations, whereby compare flag is set, the DTR is compared with the CNTR. **Data range: 00000000 – FFFFFFFF** **Example: Write 499 to DTR, W081F3**
CLEAR REG	09	W	-D, -M, -S	Clear Selected Counter Registers The following registers can be cleared to 0: 0 = MDR0 1 = MDR1 2 = CNTR 3 = STR **Data range: 0 – 3** **Example: Clear CNTR, W092**
LOAD REG	0A	W	-D, -M, -S	Load Selected Registers The following registers can be loaded: 0 = Transfer DTR to CNTR 1 = Transfer CNTR to OTR **Data range: 0 – 1** **Example: Transfer CNTR->OTR, W0A1**
THRESHOLD	0B	R, W	-D, -M, -S	Encoder Count Threshold This sets the absolute count threshold, between the previous count value and the current count value, before a new output value is reported at the selected interval rate. A value of 0 will output all values at the selected interval rate.

				Data range: 0000 – FFFF **Example: Read THRESHOLD, R0B**
INTERVAL RATE	0C	R, W	-D, -M, -S	Data Output Interval Rate This sets the data output display rate in 1.9ms steps (1/512 Hz clock). A value of 0xFFFF will disable the streaming output. A value of 0x0000 would output the data as fast as possible. For example, a value of 1 = 1.9ms delay, 2 = 3.8ms delay and so on. **Data range: 0000 – FFFF** **Example: Set 9.5ms Interval, W0C5**
TIME STAMP	0D	R, W	-D, -M, -S	Time Stamp Value The time stamp counter is a 32-bit counter incremented every 1.9ms (1/512Hz clock). It is used to time-stamp data that is saved in RAM. This counter is cleared on a power-cycle or by this command; write a 1 to this register to clear the timer. A read will return the current 32-bit time stamp value. If not reset, a counter rollover will happen every 94.5 days. **Data range: 00000000-FFFFFFFF** **Example: Reset TIME STAMP, W0D1**
READ ENCODER	0E	R, S	-D, -M, -S	Read the Current Encoder Value Read the value of the encoder. If in Quadrature mode, the encoder value will be returned as a 32-bit value. If in PWM mode, a 12/10-bit (4 character, leading 0's) value will be returned. If in Analog mode, a 10-bit value will be returned. In stream mode, the new encoder value is output at a rate set by the INTERVAL RATE and THRESHOLD parameters. A read of the encoder value will disable the streaming mode. **Data range: 00000000 – FFFFFFFF** **Example: Stream Encoder Value, S0E**
MD STEP RATE	0F	R, W	-M	MD2: Motor Step Rate Set motor step rate from 32 – 13000 steps/second. Motor rate will change in increments of 16 steps/second. (hex 20 – 32C8

				steps/second) **Data range: 00000020 – 000032C8** **Example: 1000 steps/sec, W0F3E8**
MD ACCEL	10	R, W	-M	MD2: Motor Step Acceleration Set motor step acceleration from 64 – 360000 steps/second^2. Motor acceleration will change in increments of 16 steps/second^2. (0x40 – 0x57E40 steps/second^2) **Data range: 00000040 – 00057E40** **Example: 100K steps/sec, W10186A0**
MD MOVE STEPS	11	R,W	-M	MD2: Motor Steps to Move Number of steps to move. Range + – (2^31)-1 (negative value indicates direction) **Data range: 80000001 to 7FFFFFFF** **Example: 2000 steps, W117D0**
MD JOG RATE	12	R, W	-M	MD2: Motor Jog Rate Motor rate in steps/second. Motor rate will change in increments of 16 steps/second. Range -13000 to 13000. (+/-0x32C8) **Data range: FFFFCD38 to 000032C8** **Example: 1000 steps/sec, W123E8**
MD STATUS	13	R, S	-M	MD2: Request Motor Movement Status BITS: B4 B3 B2 B1 B0 B0 = Done/Ready B1 = Moving B2 = Paused B3 = Jogging B4 = Motor Enabled In stream mode, the new MD STATUS is output upon a state change. A read of MD STATUS will cancel the streaming mode. **Data range: 0 – 1F** **Example: Read MD STATUS, W13**
VERSION	14	R	-D, -M, -S	QSB SN, Product Type and Firmware Version

				Returns the 5-digit device serial number, one-digit product type and two-digit firmware version. In the eight digit response, the first five most significant digits are the serial number, the next digit is the product type and the last two digits are the firmware version. Product type code: 0 = QSB-D 1 = QSB-M 2 = QSB-S Example, 00001201 = SN: 00001, Type: QSB-S, Version: 01 **Data range: 00000000 – FFFFFFFF** **Example: Read VERSION, R14**
EOR	15	R, W	-D, -M, -S	<u>EOR (End Of Response) Termination and Formatting</u> This command defines the type of formatting for the command response termination. Each feature is enabled with a bit=1 or disabled with a bit=0. BITS: B3 B2 B1 B0 B0 = Line Feed B1 = Carriage Return B2 = 4-byte Time Stamp appended to response B3 = Spaces between returned fields **Data range: 0 – F** **Example: All Enabled, W15F**
COMMAND	16	W	-D, -M, -S ***-D and -S*** *Data=1, 3, x0A* **-M** *Data=0-*	<u>Execute QSB Command Function</u> 0 = Motor is immediately stopped. Encoder, Digital I/O and MD Status streaming data outputs are deactivated. Motor drive status is set to the inactive state; digital I/O port is returned to the last saved state (see command #3 below).

			x0A	1 = Deactivate Encoder, Digital I/O and MD Status streaming data outputs. 2 = Activate motor drive mode; digital I/O bits 1 and 2 are reserved for motor drive. 3 = Save Parameters between power cycles: save register# 00 – 04, 08, 0B, 0C, 0F – 12, 15. Save motor drive enable state flag (command #2 above). 4 = Motor Stop - Stop the motor using the MD ACCEL rate. 5 = Motor Quit -Immediately stop the motor. 6 = Motor Pause - Pause the motor using the MD ACCEL rate. 7 = Motor Resume - Resume motor operation if previously stopped using the Motor Pause command. Use the programmed motor acceleration. 8 = Motor Move – Move the selected number of MD MOVE STEPS. 9 = Motor Jog – Jog at the selected MD JOG RATE. X0A = Communication Baud Rate Selection – (firmware version >= 13) where X = 0 – 9600 Baud 1 – 19200 Baud 2 – 38400 Baud 3 – 56000 Baud 4 – 115200 Baud 5 – 128000 Baud 6 – 230400 Baud (factory default) 7 – 256000 Baud The new Baud rate is permanently saved between power cycles

				Data range: 0 – A **Example: Save Parameters, W163** **Set 230400 Baud, W1660A**